

Title: METHOD FOR FORMING DRAM CELL BIT-LINE CONTACT

Field of Invention

[0001] The present invention relates to a method for forming the bit-line contact of DRAM cell.

Background of the Invention

[0002] DRAM is an essential element in many electronic devices. In the process of fabricating DRAM, an electronic connection between a bit-line and a drain is formed after major elements are formed on a substrate.

[0003] To fabricate the electronic connection between the bit-line and the drain, the conventional process is shown in Fig. 1 (a) to (e). The dielectric layer **103**, which is made of BPSG, is formed on the substrate **101** having a plurality of control gates **102**. Then the isolation layer **109**, which is made of TEOS, is formed on the dielectric layer **103**. Further steps include covering the isolation layer **109** with a photoresist **104** defining a contact window pattern **105**. Unprotected isolation layer **109** is etched away first with the photoresist **104** being used as a mask, and the etching is complete when the contact window **107** is formed.

[0004] As silicon-based integrated circuits shrink, the hole size defined by pattern **105** becomes smaller and smaller, which results in higher aspect ratio or higher vertical anisotropy. As known in the arts, higher vertical anisotropy presents at least two problems. First, expensive instruments are usually required. Secondly, filling a conductive material into the contact window **107** of higher aspect ratio may often cause void.

[0005] Besides, when higher vertical anisotropic etching is being performed, the shoulders of control gates 102 may be damaged and a bowl shape 106 appears. Furthermore, the size of contact window 107 formed by etching may not be easily controlled. "Crossfail" is usually caused by over-size width of the contact window 107. Insufficient width of the contact window 107 may cause void or make a drain connection insufficient. Even the prior arts have tried to overcome the problem, complicated methods or expensive instruments are usually employed.

Summary of the Invention

[0006] One aspect of the present invention provides a method for etching the dielectric layer at lower vertical anisotropy, which reduces the possibility of "crossfail" while forming the bit-line contact of DRAM.

[0007] Another aspect of the present invention provides an economical method for etching the dielectric layer at lower vertical anisotropy while forming the bit-line contact of DRAM.

[0008] Still another aspect of the present invention provides a method for etching the dielectric layer at lower vertical anisotropy, which prevents the control gates and/or their shoulders from being damaged while forming the bit-line contact of DRAM.

[0009] Yet another aspect of the present invention provides a method for etching the dielectric layer at lower vertical anisotropy, which prevents the formation of the void during the filling process of conductive material into the bit-line contact window.

[0010] A further aspect of the present invention provides a method for etching the dielectric layer at lower vertical anisotropy with easily-controlled width of contact window.

[0011] The present invention includes the following steps. A dielectric layer is formed on the substrate having a plurality of control gates. Then a patterned photoresist is formed on the dielectric layer for defining a first aperture. The isolation layer is etched away with the photoresist, and the etching is complete when a contact window is formed. Next the bit-line contact window is filled with a conductive material for forming a bit-line contact. Then the isolation layer having a second aperture for exposing a portion of the bit-line contact is formed. Filling the second aperture and a conductive layer on the isolation layer is formed.

Brief Description of the Drawings

[0012] Fig. 1(a) to Fig. 1(e) are cross-sectional view of the process of the prior art;

[0013] Fig. 2 to Fig. 8 are cross-sectional view showing processes of the present invention.

Detailed Description of the Embodiment

[0014] By referring to the Figures and the following illustrations, which are illustrative purpose rather than restrictive, it is expected that the persons skilled in the art may fully understand and utilize the advantages of the present invention. It is noted that some illustrations, elements and/or layers shown in the diagrams may be simplified or even omitted because these are well known to persons skilled in the arts.

[0015] Referring to Fig. 2, a plurality of control gates **202** are formed on the substrate **201** by any method including conventional ones. Substrate **201** is made of silicon preferably and more preferably doped silicon. In addition, the substrate **201** may have a plurality of formed regions or layers that are not shown in Fig. 2. Two control gates **202** in Fig. 2 are used to represent a plurality of control gates.

[0016] Referring to Fig. 3, the dielectric layer **203**, which is made of doped silicon dioxide preferably and more preferably BPSG, is then formed on the substrate **201**. Typical process includes the deposition and chemical vapor deposition is preferred. Optionally, the steps further include a first planarization to the dielectric layer **203**. Chemical mechanical polishing (CMP) is the preferable process for performing the planarization in this invention.

[0017] Referring to Fig. 4, a patterned photoresist **204** defining a first aperture **205** is then formed on the dielectric layer **203**. Photoresist **204** is preferably a material having substantially lower etching rate than silicon dioxide, and preferably silicon nitride. Preferred process for forming the first aperture **205** after photoresist **204** is formed is the typical etching process.

[0018] Referring to Fig. 5, the bit-line contact window **207** is then formed by etching the dielectric layer **203** with first aperture **205** being used as a pattern. Since the aspect ratio of contact window **207** of the present invention is lower than the prior art, the width and shape may be easily controlled. So that the damage of shoulder portion, "crossfail" and exposure of control gates associated with the conventional approaches are avoided.

[0019] Referring to Fig. 6, the contact window **207** is then filled with a conductive material for forming a bit-line contact **208** and the conductive layer **212** is also formed. The conductive material is preferably a metal or polysilicon, and more preferably is polysilicon or metallic materials having tungsten. The thickness of the conductive layer **212** is not restrictive but thinner is better. The conductive layer **212** is then removed by performing a second planarization, and the photoresist **204** may be removed partially, shown in Fig. 6(b), or completely, shown in Fig. 6(c). A CMP is the most preferable process for planarization.

[0020] Referring to Fig. 7, after formation of the bit-line contact **208**, the isolation layer **209** having a second aperture **210** is formed for exposing a portion of the bit-line contact **208**. TEOS is preferred for the isolation layer **209**. Etching is the preferable process for forming the second aperture **210**.

[0021] Referring to Fig. 8, the conductive layer **211** is formed and, at the same time, the second aperture **210** is filled with the conductive material. The conductive material is preferably a metal or polysilicon, and more preferably are metallic materials having tungsten or polysilicon. At the end of process shown in Fig. 8, the bit-line contact of DRAM is formed on substrate **201**.

[0022] By means of the above detailed descriptions of the subject invention, it is the expectation that these above-mentioned illustrations are not intended to be construed in a limiting sense. Instead, it should be well understood that any equivalent variation and equivalent arrangement are covered within the spirit and scope to be protected by the following claims and their equivalences.